# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## M.TECH. VLSI SYSTEM DESIGN
## COURSE STRUCTURE & SYLLABI

### SEMESTER– I

| S. No. | Course codes | Course Name | Category | Hours per week | | | Credits |
|---|---|---|---|---|---|---|---|
| | | | | L | T | P | |
| **1.** | 25G3D57101 | CMOS Analog IC Design | PC | 3 | 0 | 0 | 3 |
| **2.** | 25G3D57102 | CMOS Digital IC Design | PC | 3 | 0 | 0 | 3 |
| **3.** | | **Program Elective– 1** | PE | 3 | 0 | 0 | 3 |
| | 25G3D57103a | Microchip Fabrication Techniques | | | | | |
| | 25G3D57103b | Scripting Languages for VLSI | | | | | |
| | 25G3D57103c | CAD for VLSI | | | | | |
| **4.** | | **Program Elective–II** | PE | 3 | 0 | 0 | 3 |
| | 25G3D57104a | Device Modeling | | | | | |
| | 25G3D57104b | FPGA Architectures and Applications | | | | | |
| | 25G3D57104c | ASIC Design | | | | | |
| **5.** | 25G3D57105 | CMOS Analog IC Design Lab | PC | 0 | 0 | 4 | 2 |
| **6.** | 25G3D57106 | CMOS Digital IC Design Lab | PC | 0 | 0 | 4 | 2 |
| **7.** | 25G3DRM101 | Research Methodology and IPR | MC | 2 | 0 | 0 | 2 |
| **8.** | 25G3DRT101 | RTL Synthesis, Simulation and Verification | SE | 0 | 1 | 2 | 2 |
| **9.** | | **Audit Course–I** | AC | 2 | 0 | 0 | 0 |
| | 25G3DAC101a | English for Research paper writing | | | | | |
| | 25G3DAC101b | Disaster Management | | | | | |
| | 25G3DAC101c | Indian Knowledge System | | | | | |
| **Total** | | | | | | | **20** |

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## CMOS ANALOG IC DESIGN

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57101 | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Design MOSFET based analog integrated circuits. |
| CO2: | Analyze analog circuits at least to the first order. |
| CO3: | Appreciate the trade-offs involved in analog integrated circuit design. |
| CO4: | Understand and appreciate the importance of noise and distortion in analog circuits. |
| CO5: | Analyze complex engineering problems critically in the domain of analog IC design for conducting research. |

| UNIT-I: Basic MOS Device Physics |
|---|
| General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor, Short Channel Effects and Device Models, Single Stage Amplifiers– Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage. |
| **UNIT-II: Differential Amplifiers** |
| Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors–Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit |
| **UNIT-III: Frequency Response of Amplifiers** |
| General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise–Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs. |
| **UNIT-IV: Feedback Amplifiers** |
| General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers–General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common–Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation. |
| **UNIT-V: Operational Amplifiers** |
| One stage op-amp, two stage op-amp, gain boosting, common mode feedback, input range limitations, slew rate, PSRR, compensation of two stage, Slewing in Two Stage Op-Amp, Compensation Techniques. Design Procedure for 2-Stage Op-Amp. |

**Textbooks:**


1. B. Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition2016.
2. Paul. R. Gray & Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.


**Reference Books:**


1. T. C. Carusone, D. A. Johns & K. Martin, "Analog Integrated Circuit Design",2nd Edition, Wiley,2012.
2. P.E. Allen & D.R. Holberg, "CMOSAnalogCircuitDesign",3rd Edition, Oxford University Press, 2011.
3. R. Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rdEdition, Wiley, 2010.
4. Adel S. Sedra, Kenneth C. Smith, Arun, "MicroelectronicCircuits",6th Edition, Oxford University Press

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## CMOS DIGITAL IC DESIGN

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57102 | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS. |
| CO2: | Estimate Delay and Power of Adders circuits. |
| CO3: | Classify different semiconductor memories. |
| CO4: | Analyze, design and implement combinational and sequential MOS logic circuits. |
| CO5: | Analyze complex engineering problems critically in the domain of digital IC design for conducting research. |

| UNIT-I: MOS Design Pseudo NMOS Logic |
|---|
| Inverter, Inverter threshold voltage, output high voltage, Output Low voltage, Gain at gate Threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic. |
| **UNIT-II: Combinational MOS Logic Circuits** |
| MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates. |
| **UNIT-III: Sequential MOS Logic Circuits** |
| Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop |
| **UNIT-IV: Dynamic Logic Circuits** |
| Basic principle, Voltage Bootstrapping, Synchronous dynamic pass Transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits. |
| **UNIT-V: Semiconductor Memories** |
| Types, RAM array organization, DRAM– Types, Operation, Leakage currents in DRAM cell and Refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash. |

**Text books:**


1. Neil Weste, David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.


**Reference Books:**


1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective –Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits–A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## MICROCHIP FABRICATION TECHNIQUES

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57103a | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Understand various stages of fabrication. |
| CO2: | Understand Various packaging techniques and Design rules. |
| CO3: | Classify various thin films and its characteristics. |
| CO4: | Differentiate between various Chemical Vapor Deposition (CVD) methods such as LPCVD and PECVD. |
| CO5: | Explain the functions and characteristics of chip packaging in semiconductor devices. |

| UNIT-I: Introduction to Processing |
|---|
| Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, clean room construction. |
| **UNIT-II: Photolithography** |
| Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping. |
| **UNIT-III: Diffusion & Ion Implantation** |
| Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2. |
| **UNIT-IV: Film Depositions and Growth** |
| Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy. |
| **UNIT-V: Yield &Packaging** |
| **Yield:** Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.<br>**Packaging:** Chip characteristics, package functions, package operations. |

**Textbooks:**

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. Plummer, J.D., Deal, M.D. and Griffin, P.B., “Silicon VLSI Technology: Fundamentals, Practice and Modeling”, 3rd Ed., Prentice-Hall, 2000.

**Reference Books:**

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book Company, NY, 1988

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## SCRIPTING LANGUAGES FOR VLSI

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57103b | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Gain fluency in programming with scripting languages |
| CO2: | Create and run scripts using PERL/TCL/PYTHON in CAD Tools |
| CO3: | Demonstrate the use of PERL/PYTHON/ TCL in developing system and web applications |
| CO4: | Develop a real time project using PERL/PYTHON. |
| CO5: | Analyze security issues in TCL applications and Utilize Python modules to organize code and extend functionality |

| UNIT-I Introduction to Scripts and Scripting |
|---|
| Basics of Linux, Origin of Scripting languages, scripting today, Characteristics and uses of scripting languages. |
| **UNIT-II PERL** |
| **PERL:** Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments. |
| **UNIT-III Advanced PERL** |
| Finer points of Looping, Subroutines, Using Pack and Unpack, working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects and modules in action, Tied variables, interfacing to the operating systems, Security issues. |
| **UNIT-IV TCL** |
| The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code. |
| **UNIT-V Advanced TCL** |
| The eval, source, exec and up-level commands, Libraries and packages, Namespaces, trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, TCL and TK integration.<br>PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements, functions, Built-in functions and Methods, Modules in PYTHON, Exception Handling. |

**Text books:**


1. The World of Scripting Languages- David Barron, Wiley Student
2. Web Programming, Steve Holden and David Beazley, New Riders Publications.


**Reference Books:**


1. TCL/TK: A Developer's Guide- Clif Flynt, Morgan Kaufmann Series.
2. Core PYTHON Programming, Chun, Pearson Education.
3. Learning Perl, Randal L. Schwartz, O' Reilly publications 6th edition.
4. Linux: The Complete Reference", Richard Peterson McGraw Hill Publications, 6thEdition

# St. Johns College of Engineering and Technology

## (AUTONOMOUS)

### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## CAD FOR VLSI

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57103c | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Establish comprehensive understanding of the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification |
| CO2: | Demonstrate knowledge and understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement. |
| CO3: | Practice the application of fundamentals of VLSI technologies |
| CO4: | Optimize the implemented design for area, timing and power by applying suitable constraints. |
| CO5: | Apply knowledge of partitioning and routing to optimize FPGA design performance. |

| **UNIT-I: Introduction** |
|---|
| VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles |
| **UNIT-II: Partitioning** |
| Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing |
| **UNIT-III: Floor Planning** |
| Floor Planning – Problem formulation, Classification of floor planning algorithms, constraint-based floor planning, Rectangular Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments. |
| **UNIT-IV: Placement and Routing** |
| **Placement and Routing:** Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.<br>**Global Routing and Detailed Routing**: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms. |
| **UNIT-V: Physical Design Automation of FPGAs and MCMs** |
| FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle. |

**Text books:**


1. Algorithms for VLSI Physical Design Automation by Naveed Shervani,3rdEdition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011


**Reference Books:**


1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition

# St. Johns College of Engineering and Technology

## (AUTONOMOUS)

### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## DEVICE MODELLING

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| 25G3D57104a | PE | L | T | P | C | CIA | SEE | Total |
| | | 3 | 0 | 0 | 3 | 30 | 70 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Understand the physics of 2-terminal MOS operation and its characteristics |
| CO2: | Understand the physics of 4-terminal MOSFET operation and its characteristics. |
| CO3: | Analyze the SOI MOSFET electrical characteristics. |
| CO4: | Analyze the impact of scaling on MOSFET performance and limitations. |
| CO5: | Apply SOI MOSFET concepts to advanced semiconductor device design challenges. |

| UNIT-I: 2-terminal MOS device |
|---|
| Threshold voltage modeling (ideal case as well as considering the effects of Φms and Dit.). |
| **UNIT-II: C-V characteristics** |
| C-V characteristics (ideal case as well as taking into account the effects of Qf,Φms and Dit); MOS capacitor<br>as a diagnostic tool (measurement of non-uniform doping profile, estimation of Qf, Φms and Dit) |
| **UNIT-III: 4-terminal MOSFET** |
| Threshold voltage (considering the substrate bias); above threshold I-V Modeling (SPICE level 1, 2, 3 and 4). |
| **UNIT-IV: Sub threshold current model** |
| Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modeling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model) |
| **UNIT-V: SOI MOSFET** |
| SOI MOSFET: Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; high-K gate dielectrics. |

**Textbooks:**

1. S. M. Sze, Physics of Semiconductor Devices, (2e), WileyEastern,1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd 2017.

**Reference Books:**

1. Y. P. Tsividis, Operation and Modeling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
3. J.P. Colinge, "Fin FET sand Other Multi-Gate Transistors," Springer.2009

# St. Johns College of Engineering and Technology

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### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## FPGA ARCHITECTURES AND APPLICATIONS

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57104b | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Acquire knowledge about various architectures and device technologies of PLD's. |
| CO2: | Comprehend FPGA Architectures |
| CO3: | Analyze System level Design and their application for Combinational and Sequential Circuits. |
| CO4: | Familiarize with Anti-Fuse Programmed FPGAs. |
| CO5: | Apply knowledge of this subject for various design applications. |

| UNIT-I: Introduction to Programmable Logic Devices |
|---|
| Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/ Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation |
| **UNIT-II: Field Programmable Gate Arrays** |
| Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs. |
| **UNIT-III: SRAM Programmable FPGAs** |
| Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures |
| **UNIT-IV: Anti- Fuse Programmed FPGAs** |
| Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures. |
| **UNIT-V: Design Applications** |
| General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture. |

**Text books:**


1. Field Programmable Gate Array Technology-Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design- Charles H. Roth Jr, Lizy Kurian John, Cengage Learning.


**Reference Books:**


1. Field Programmable Gate Arrays- John V. Old field, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays –Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs- Ian Grout, Elsevier, Newness.
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## ASIC DESIGN

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57104c | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Understand different types of ASICs and their libraries. |
| CO2: | Understand about programmable ASICs, I/O modules and their interconnects. |
| CO3: | Familiarize different methods of software ASIC design their simulation, testing and construction of ASICs. |
| CO4: | Implement synthesis using Verilog and VHDL for FSMs, memory, and controller designs. |
| CO5: | Analyze physical design aspects using CAD tools, including system partitioning and ASIC size estimation. |

| **UNIT-I: Introduction to ASICs** |
|---|
| Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design |
| **UNIT-II: Programmable ASICs and Programmable ASIC Logic Cells** |
| The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max. |
| **UNIT-III: I/O Cells and Interconnects & Programmable ASIC Design Software** |
| DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC. |
| **UNIT-IV: Low Level Design Entry and Logic Synthesis** |
| Schematic Entry, Low level Design Languages, PLA Tools, EDIF, A logic synthesis example, A Comparator/MUX, Inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the Viterbi decoder. |
| **UNIT-V: Simulation, Test and ASIC Construction** |
| Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, The importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning, Estimating ASIC Size, Power Dissipation, FPGA Partitioning, Partitioning Methods. |

**Text books:**

1. Michael John Sebastian Smith, “Application Specific Integrated Circuits”, Pearson Education, 2003.
2. L. J. Herbst, “Integrated Circuit Engineering”, Oxford Science Publications, 1996.

**Reference Books:**

1. Himanshu Bhatnagar, “Advanced ASIC Chip Synthesis using Synopsis Design Compiler”, 2nd Edition, Kluwer Academic, 2001.

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## CMOS ANALOG IC DESIGN LAB

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57105 | PC | 0 | 0 | 4 | 2 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Explain the VLSI Design Methodologies using VLSI design tool. |
| CO2: | Grasp the significance of various CMOS analog circuits in full-custom IC Design flow |
| CO3: | Explain the Physical Verification in Layout Design |
| CO4: | Fully appreciate the design and analyze of analog and mixed signal simulation |
| CO5: | Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation |

**List of Experiments:**

- The students are required to design and implement using CMOS Technology.
- The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Two stage Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

**Lab Requirements:**

**Software:**

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

**Hardware:**

Personal Computer with necessary peripherals, configuration and operating System.

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## CMOS DIGITAL IC DESIGN LAB

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| **Course Code** | **Category** | **Hours/Week** | | | **Credits** | **Maximum Marks** | | |
| **25G3D57106** | **PC** | **L** | **T** | **P** | **C** | **CIA** | **SEE** | **Total** |
| | | 0 | 0 | 4 | 2 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Explain the VLSI Design Methodologies using any VLSI design tool. |
| CO2: | Grasp the significance of various design logic Circuits in full-custom. |
| CO3: | Explain the Physical Verification in Layout Extraction. |
| CO4: | Fully appreciate the design and analyze of CMOS Digital Circuits. |
| CO5: | Apply circuit simulation tools to evaluate performance parameters (delay, power, area) of CMOS designs. |

**List of Experiments:**

The students are required to design and implement the Circuit and Layout of any **Twelve** Experiments using CMOS Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

**Lab Requirements:**

**Software:**

Mentor Graphics Tool/ Cadence/ Synopsys/ Industry Equivalent Standard Software

**Hardware:**

Personal Computer with necessary peripherals, configuration and operating System.

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## RESEARCH METHODOLOGY AND INTELLECTUAL PROPERTY RIGHTS

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3DRM101 | MC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Recall key concepts and terminology related to research design, data collection, and intellectual property rights. |
| CO2: | Explain the importance of research design and data analysis in research studies, and describe the concept of intellectual property rights. |
| CO3: | Design a research study, including data collection and analysis methods, and apply intellectual property rights principles to protect research findings. |
| CO4: | Analyze research studies to identify strengths and limitations, and evaluate the effectiveness of data collection and analysis methods. |
| CO5: | Develop a comprehensive research plan, including a detailed research design, data collection and analysis methods, and a plan for protecting intellectual property. |

| UNIT-I: Fundamentals of Research Methodology |
|---|
| Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences |
| **UNIT-II: Data Collection and Sources** |
| Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection. |
| **UNIT-III: Data Analysis and Reporting** |
| Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals. |
| **UNIT-IV: Understanding Intellectual Property Rights** |
| Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance. |
| **UNIT-V: Patents** |
| Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents. |

**Text books:**


1. Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004
2. Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007.


**Reference Books:**


1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education 11e (2012).
2. Ranjit Kumar, Research Methodology: A Step-by-Step Guide for Beginners. David Hunt,

Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
3. Deborah E. Bouchoux, Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.
4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.
6. Peter Elbow, Writing with Power, Oxford University Press, 1998.

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## RTL SYNTHESIS, SIMULATION AND VERIFICATION

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3DRT101 | SE | 2 | 0 | 0 | 2 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Demonstrate the process steps required for simulation /synthesis |
| CO2: | Design and simulate various combinational and sequential circuits |
| CO3: | Develop an RTL code for various real time applications. |
| CO4: | Synthesize / Simulate an RTL code for several digital design |
| CO5: | Build and verify various digital circuits. |

**Module 1 – Introduction to RTL Design**

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (System Verilog/VHDL basics).
- Lab:
  1. Write synthesizable Verilog/ System Verilog code for:
     a) Half Adder, Full Adder
     b) 4-bit Ripple Carry Adder
     c) 4-bit Synchronous Counter (Up/Down)
  2. FSM Design: Sequence Detector (e.g., detect “1011”).

**Module 2 – RTL Synthesis**

- Synthesis concepts: mapping RTL to gate-level net list.
- Constraints: clock, area, power.
- Lab:
  1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool
  2. Generate gate-level net list and analyze area, delay, power reports.
  3. Apply constraints (clock, timing) and observe impact on synthesis results.

**Module 3 – Simulation**

- Functional vs. Timing simulation.
- Test bench creation, waveforms, debugging.
- Lab: Run simulations
  1. Develop test benches for:
     a) 4-bit ALU (add, sub, AND, OR).
     b) Universal Shift Register.
  2. Perform functional simulation using EDA tools
  3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

**Module 4 – Verification**

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- Lab: Writing simple verification test benches.
  1. Write self-checking test benches for combinational and sequential circuits.
  2. Use assertion-based verification (System Verilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
  3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

**Module 5 – Case Study & Mini Project**

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- Lab: Design, synthesize, simulate, and verify a **digital subsystem** such as:
  1. UART Transmitter/Receiver
  2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)
  3. FIFO Buffer with full/empty flags

**Textbooks / References**

1. Samir Palnitkar – Verilog HDL: A Guide to Digital Design and Synthesis.
2. Michael Ciletti – Advanced Digital Design with the Verilog HDL.
3. Chris Spear & Greg Tumbush – System Verilog for Verification.
4. David Rich – Design and Verification with System Verilog.

**Suggested reading:**

1. Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall 2003.
2. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx, 2011.
3. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books, 2002.

St. Johns College of Engineering and Technology
(AUTONOMOUS)
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

# AUDIT COURSE-I

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)
### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## ENGLISH FOR RESEARCH PAPER WRITING

| IM. Tech–I Semester | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3DAC101a | AC | 2 | 0 | 0 | 0 | 40 | 0 | 40 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Recall the key language aspects and structural elements of academic writing in research papers. |
| CO2: | Explain the importance of clarity, precision, and objectivity in research writing. |
| CO3: | Apply critical reading strategies and advanced grammar skills to analyze and write research papers. |
| CO4: | Analyze research articles and identify the strengths and limitations of different methodologies. |
| CO5: | Evaluate the effectiveness of different language and technology tools in research writing, including AI assisted tools and plagiarism detection software. |

| UNIT-I: Fundamentals of Academic English |
|---|
| Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills – Framing Title and Sub-headings. |
| **UNIT-II: Reading Skills for Researchers** |
| Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes. |
| **UNIT-III: Grammar Refinement for Research Writing** |
| Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures -Active-Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences |
| **UNIT-IV: Mastery in Refining Written Content/Editing Skills** |
| Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision – Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing. |
| **UNIT-V: Technology and Language for Research** |
| Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing – Assistance in Generating Citations and References - Plagiarism and Ethical Considerations – Tools and Awareness – Fair Practices |

**Textbooks:**


1. 1.Bailey. S. Academic Writing: A Handbook for International Students. London and New York: Routledge,2015.
2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.


**Reference Books:**


1. Craswell, G. Writing for Academic Success, Sage Publications, 2004.
2. Peter Elbow, Writing With Power, E-book, Oxford University Press, 2007.
3. Oshima, A. & Hogue, A. Writing Academic English, Addison-Wesley, New York, 2005.
4. Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills and Tasks. Michigan University Press, 2012.
5. Goldbort R. Writing for Science, Yale University Press (available on Google Books), 2006
6. Day R. How to Write and Publish a Scientific Paper, Cambridge University Press, 2006

# St. Johns College of Engineering and Technology

## (AUTONOMOUS)

### DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## DISASTER MANAGEMENT

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3DAC101b | AC | 2 | 0 | 0 | 0 | 40 | 0 | 40 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Define and distinguish between hazards and disasters, and explain their types, nature, and impacts. |
| CO2: | Identify and map disaster-prone areas in India and understand the epidemiological consequences of disasters. |
| CO3: | Assess the economic, social, and ecological repercussions of major natural and man-made disasters. |
| CO4: | Demonstrate knowledge of disaster preparedness tools such as remote sensing, meteorological data, risk evaluation, and community awareness. |
| CO5: | Apply risk assessment methods and propose disaster risk reduction strategies at local, national, and global levels. |

| UNIT-I: Introduction |
|---|
| Disaster - Definition, Factors and Significance - Difference Between Hazard and Disaster - Natural and Man-made Disasters - Difference, Nature, Types and Magnitude - Disaster Prone Areas in India - Study of Seismic Zones - Areas Prone to Floods and Droughts, Landslides and Avalanches - Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami - Post Disaster Diseases and Epidemics. |
| **UNIT-II: Repercussions of Disasters and Hazards** |
| Economic Damage - Loss of Human and Animal Life - Destruction of Ecosystem - Natural Disasters - Earthquakes, Volcanism, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster - Nuclear Reactor Meltdown - Industrial Accidents - Oil Slick sand Spills - Outbreaks of Disease and Epidemics War and Conflicts |
| **UNIT-III: Disaster Preparedness and Management** |
| Preparedness - Monitoring of Phenomena - Triggering a Disaster or Hazard - Evaluation of Risk Application of Remote Sensing - Data from Meteorological and Other Agencies - Media Reports-Governmental and Community Preparedness. |
| **UNIT-IV: Risk Assessment** |
| Disaster Risk -Concept and Elements, Disaster Risk Reduction - Global and National Disaster Risk Situation -Techniques of Risk Assessment – Global Co-Operation in Risk Assessment and Warning - People's participation in Risk Assessment – Strategies for Survival. |
| **UNIT-V: Disaster Mitigation** |
| Meaning, Concept and Strategies of Disaster Mitigation - Emerging Trends in Mitigation - Structural Mitigation and Non- Structural Mitigation - Programs of Disaster Mitigation in India |

**Text books**

1. Gupta, H. K. Disaster Management. Universities Press, 2003
2. Singh, R. B. Natural Hazards and Disaster Management. Rawat Publications, 2006.

**Reference Books**

1. Coppola, D. P. (2020). Introduction to International Disaster Management (4th ed.). Elsevier.
2. Shaw, R., & Izumi, T. (2022). Science and Technology in Disaster Risk Reduction in Asia. Springer.
3. Wisner, B., Gaillard, J. C., & Kelman, I. (2021). Handbook of Hazards and Disaster Risk Reduction and Management (2nd ed.). Routledge.
4. Saini, V. K. (2021). Disaster Management in India: Policy, Issues and Perspectives. Sage India.

5. Kelman, I. Disaster by Choice: How Our Actions Turn Natural Hazards into Catastrophes, Oxford University Press, 2022
6. Sahni, P. & Dhameja, A. Disaster Mitigation: Experiences and Reflections. Prentice Hall of India, 2004.

# St. Johns College of Engineering and Technology
## (AUTONOMOUS)

## ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE

| I M. Tech–I Semester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| Course Code | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3AAC101c | AC | 2 | 0 | 0 | 0 | 40 | 0 | 40 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Define and explain the concept of traditional knowledge, its nature, characteristics, and scope. |
| CO2: | Understand the need for protecting traditional knowledge and its significance in the global economy. |
| CO3: | Explain the legal framework and policies related to traditional knowledge protection. |
| CO4: | Apply traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology. |
| CO5: | Analyze the importance of traditional knowledge in various contexts, including its historical impact and social change . |

| UNIT-I |
|---|
| Introduction to traditional knowledge - Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge - Traditional knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge |
| **UNIT-II** |
| Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK. |
| **UNIT-III** |
| Legal frame work and TK - A) The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B) The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003. |
| **UNIT-IV** |
| Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge. |
| **UNIT-V** |
| Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK |

**Text books**


1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. Introduction to Indian Knowledge System: Concepts and Applications, PHI Learning Pvt.Ltd. Delhi, 2022.
2. Basanta Kumar Mohanta and Vipin Kumar Singh, Traditional Knowledge System and Technology in India, Pratibha Prakashan 2012.


**Reference Books**


1. Pride of India: A Glimpse into India's Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. "On Astronomy in Ancient India", Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. Indian Astronomy: A Source Book, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. History of Technology in India, Vol. I, Indian National Science Academy, New

Delhi, 1997.
5. Acarya, P.K. Indian Architecture, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. Public Administration in Ancient India, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh, Indian Knowledge Systems Vol – I & II, Indian Institute of Advanced Study, Shimla, H.P., 2022

# St.JohnsCollegeofEngineeringandTechnology
## (AUTONOMOUS)
### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## M.TECH. VLSI SYSTEM DESIGN
## COURSE STRUCTURE&SYLLABI
### SEMESTER – II

| S. No. | Course codes | Course Name | Category | Hours per week | | | Credit |
|---|---|---|---|---|---|---|---|
| | | | | L | T | P | |
| 1. | 25G3D57201 | CMOS Mixed Signal IC Design | PC | 3 | 0 | 0 | 3 |
| 2. | 25G3D57202 | Physical Design Automation | PC | 3 | 0 | 0 | 3 |
| 3. | 25G3D57203a<br>25G3D57203b<br><br>25G3D57203c | **Program Elective – III**<br>SoC Testing and Verification<br>Semiconductor Memory Design and Testing<br><br>Advanced VLSI interconnects | PE | 3 | 0 | 0 | 3 |
| 4. | 25G3D57204a<br>25G3D57204b<br>25G3D57204c | **Program Elective – IV**<br>Low Power VLSI Design<br>Algorithms for VLSI Design<br>VLSI Signal Processing | PE | 3 | 0 | 0 | 3 |
| 5. | 25G3D57205 | CMOS Mixed Signal IC Design Lab | PC | 0 | 0 | 4 | 2 |
| 6. | 25G3D57206 | Physical Design Automation Lab | PC | 0 | 0 | 4 | 2 |
| 7. | 25G3D57207 | Quantum Technologies and Applications | MC | 2 | 0 | 0 | 2 |
| 8. | 25G3D57208 | Comprehensive Viva Voce | PC | 0 | 0 | 0 | 2 |
| 9. | 25G3DAC201a<br>25G3DAC201b<br>25G3DAC201c | **Audit Course – II**<br>Pedagogy Studies<br>Stress Management for Yoga<br>Personality Development through Life Enlightement Skills | AC | 2 | 0 | 0 | 0 |
| | | **Total** | | | | | **20** |

# St.JohnsCollegeofEngineeringandTechnology
## (AUTONOMOUS)
### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## CMOS MIXED SIGNAL IC DESIGN

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57201 | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Demonstrate first order filter with least interference |
| CO2: | Extend the concept of phase locked loop for designing PLL application with minimum jitter by Considering non ideal effects. |
| CO3: | Design different D/A converters, Decoders ,Code converters for real time applications |
| CO4: | Design different A/D for real time applications |
| CO5: | Design different modulators, demodulators and different filter for real time applications |

| UNIT-I: Switched Capacitor Circuits |
|---|
| Introduction to Switched Capacitor circuits-basic building blocks, Operation and Analysis, Non-ideal effectsinswitchedcapacitorcircuits,Switchedcapacitorintegrators,firstorderfilters,Switchsharing, Bi quad filters. |
| **UNIT-II: Phased Lock Loop (PLL)** |
| Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/C P non-idealities, Jitter in PLLs, Delay locked loops, applications |
| **UNIT-III: Data Converter** |
| Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters-Decoder basedconverters,Binary-Scaledconverters,Thermometer-codeconverters,Hybridconverters |
| **UNIT-IV: A to D Converters** |
| Nyquist Rate A/D Converters Successive approximation converters, Flash converter, Two-step A/D converters,InterpolatingA/Dconverters,FoldingA/Dconverters,PipelinedA/Dconverters,SigmaDelta A/D converters, Time-interleaved converters. |
| **UNIT-V:Oversampling Converters** |
| Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A |

**Textbooks:**


1. DesignofAnalogCMOSIntegratedCircuits-BehzadRazavi,TMHEdition,2002
2. CMOS Analog Circuit Design-PhilipE. Allen and Douglas R.Holberg, Oxford University Press, International Second Edition/Indian Edition, 2010.
3. AnalogIntegratedCircuitDesign-DavidA.Johns,KenMartin,WileyStudentEdition,2013


**ReferenceBooks:**


1. CMOS Integrated Analog-to-Digital and Digital-to-Analog converters- Rudy Van De Plassche, Kluwer Academic Publishers, 2003
2. UnderstandingDelta-SigmaDataconverters-RichardSchreier,WileyInterscience,2005.
3. CMOSMixed-SignalCircuitDesign-R.JacobBaker,WileyInterscience,2009

# St.JohnsCollegeofEngineeringandTechnology
## (AUTONOMOUS)
### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## PHYSICAL DESIGN AUTOMATION

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57202 | PC | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Understand relation between automation algorithms and constraint sposed by VLSItechnology. |
| CO2: | Adopt algorithms to meet critical design parameters. |
| CO3: | Design area efficient logics by employing different routing algorithms and shape functions. |
| CO4: | Simulate and synthesis different combinational and sequential logics. |
| CO5: | Understand the different levels of high level synthesis. |

| UNIT-I:VLSIDesignAutomationTools |
|---|
| Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools. |
| **UNIT-II: Layout** |
| Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuitrepresentation,Wirelength estimation, Placement algorithms, Partitioning algorithms. |
| **UNIT-III: Floor planning and routing** |
| Floorplanningconcepts,Shapefunctionsandfloorplanningsizing,Localrouting,Arearouting,Channel routing, global routing and its algorithms. |
| **UNIT-IV:SimulationandLogicSynthesis** |
| Gatelevelandswitchlevelmodelingandsimulation,Introductiontocombinationallogicsynthesis, ROBDDprinciples,implementation,constructionandmanipulation,Twolevellogicsynthesis. |
| **UNIT-V:High-LevelSynthesis** |
| Hardwaremodelforhighlevelsynthesis,internalrepresentationofinputalgorithms,Allocation,assignment andscheduling,schedulingalgorithms,Aspectsofassignment,Highleveltransformations. |

**Textbooks:**

1. S.H.Gerez,AlgorithmsforVLSIDesignAutomation,JohnWiley,1998.
2. N.A.Sherwani,AlgorithmsforVLSIPhysicalDesignAutomation,(3/e),Kluwer,1999.

**ReferenceBooks:**

1. S.M.Sait,H.Youssef,VLSIPhysicalDesignAutomation,Worldscientific,1999.
2. M.Sarrafzadeh,IntroductiontoVLSIPhysicalDesign,McGrawHill(IE),1996

# St.JohnsCollegeofEngineeringandTechnology

## (AUTONOMOUS)

### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## SoC TESTING AND V ERIFICATION

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| 25G3D57203a | PE | L | T | P | C | CIA | SEE | Total |
| | | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | UnderstandtheconceptsoffaultsandtestinginSoC |
| CO2: | Implementthefaultsusingsimulationtools |
| CO3: | Understandtheconceptsofcontrollabilityandobservability |
| CO4: | AnalyzeBISTsystems |
| CO5: | UnderstandSystemConfigurationwithBoundary Scan |

| UNIT-I:Introductionto Testing |
|---|
| TestingPhilosophy,RoleofTesting,DigitalandAnalogVLSITesting,VLSITechnologyTrendsaffecting Testing, Types of Testing, Fault Modeling: Defects, Errors and Faults, Functional Versus Structural Testing,LevelsofFaultModels,SingleStuck-atFault. |
| **UNIT-II:LogicandFaultSimulation** |
| SimulationforDesignVerificationandTestEvaluation,ModelingCircuitsforSimulation,Algorithmsfor True-value Simulation, Algorithms for Fault Simulation. |
| **UNIT-III:TestabilityMeasures** |
| SCOAPControllabilityandObservablity,HighLevelTestabilityMeasures,DigitalDFTandScanDesign: Ad-Hoc DFT Methods, Scan Design, Partial-Scan Design, Variations of Scan. |
| **UNIT-IV:Built-InSelf-Test** |
| The Economic Case for BIST, Random Logic BIST: Definitions, BIST Process, Pattern Generation, ResponseCompaction,Built-InLogic BlockObservers,Test-Per-Clock,Test-Per-ScanBISTSystems, CircularSelfTestPathSystem,MemoryBIST,DelayFaultBIST. |
| **UNIT-V: BoundaryScanStandard** |
| Motivation, SystemConfiguration withBoundaryScan:TAP Controller andPort, BoundaryScanTest Instructions,PinConstraintsoftheStandard,Boundary ScanDescriptionLanguage:BDSLDescription Components,PinDescriptions. |

**Textbooks:**

1. M.L.Bushnell,V.D.Agrawal,"EssentialsofElectronicTesting forDigital,MemoryandMixed Signal VLSI Circuits", Kluwer Academic Pulishers.
2. M.Abramovici,M.A.BreuerandA.DFriedman,"DigitalSystemsandTestableDesign",Jaico Publishing House.

**ReferenceBooks:**

1. P.K.Lala,"DigitalCircuitsTestingandTestability",AcademicPress.

# St.JohnsCollegeofEngineeringandTechnology
## (AUTONOMOUS)
### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## SEMICONDUCTOR MEMORY DESIGN AND TESTING

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| 25G3D57203b | PE | L | T | P | C | CIA | SEE | Total |
| | | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | Getcompleteknowledgeregardingdifferenttypesof RAM memories,theirarchitecturaland different packing techniques of memories. |
| CO2: | Getcompleteknowledgeregardingdifferenttypesofnon-volatilememories,their architectural anddifferentpackingtechniquesof memories. |
| CO3: | Buildfaultmodelsformemorytesting. |
| CO4: | Analyzedifferentparametersthatleadmalfunctioningofmemories. |
| CO5: | Designreliablememorieswithefficientarchitecturetoimproveprocessestimesandpower. |

| UNIT-I:RandomAccessMemory Technologies |
|---|
| SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, AdvancedSRAM architectures andtechnologies, Application specific SRAMs, DRAM– DRAM technology development, CMOS DRAM, DRAM cell theoryandadvancedcellstructures,BICMOSDRAM,softerrorfailureinDRAM,AdvancedDRAM designandarchitecture,ApplicationspecificDRAM. |
| **UNIT-II:Non-volatileMemories** |
| MaskedROMs,HighdensityROM,PROM,BipolarROM,CMOSPROMS,EPROM,Floatinggate EPROMcell,OnetimeprogrammableEPROM, EEPROM,EEPROMtechnologyandarchitecture,Non- volatile SRAM, Flash Memories(EPROM or EEPROM), advanced Flash memory architecture |
| **UNIT-III: MemoryFaultModelingTestingandMemoryDesign forTestabilityandFault Tolerance** |
| RAMfaultmodeling,Electricaltesting,PseudoRandomtesting,MegabitDRAMTesting,non-volatile memory modelingandtesting, IDDQ fault modelingandtesting, Application specific Memorytesting, RAM fault modeling, BIST techniques for memory. |
| **UNIT-IV:SemiconductorMemoryReliabilityandRadiationEffects** |
| General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory characteristics, Radiation Hardness Assuranceand Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures. |
| **UNIT-V:AdvancedMemoryTechnologiesandHigh-densityMemoryPackingTechnologies** |
| FerroelectricRAMs(FRAMs),GaAsFRAMs,Analogmemories,magnetoresistiveRAMs(MRAMs), Experimental memory devices, Memory Hybrids and MCMs(2D), Memory Stacks andMCMs(3D), MemoryMCM testingandreliabilityissues, Memorycards, HighDensity Memory PackagingFuture Directions. |

**Textbooks:**

**1.** SemiconductorMemoriesTechnology–AshokK.Sharma,2002,Wiley.
2. AdvancedSemiconductorMemories –Architecture,DesignandApplications -AshokK. Sharma, 2002, Wiley.

**ReferenceBooks:**

1. ModernSemiconductorDevicesforIntegratedCircuits–ChenmingCHu,FirstEdition. Prenticeall.

# St.JohnsCollegeofEngineeringandTechnology

## (AUTONOMOUS)

### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## ADVANCED VLSI INTERCONNECTS

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| 25G3D57203c | PE | L | T | P | C | CIA | SEE | Total |
| | | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | Understand the fundamentals of VLSI interconnects and their impact on chip performance. |
| CO2: | Analyze resistance, capacitance, and delay associated with on-chip interconnects. |
| CO3: | Evaluate signal integrity issues such as crosstalk, noise, and power dissipation in VLSI interconnects |
| CO4: | Study modeling techniques for interconnect delay and performance in deep submicron technologies. |
| CO5: | Apply advanced interconnect technologies and optimization techniques in modern VLSI design |

| UNIT I: Introduction to Interconnects |
|---|
| Interconnect scaling, parasitic resistance, capacitance, and inductance modeling. Interconnect materials (copper, aluminum) and dielectric materials (low-k). |
| **UNIT II: Interconnect Modeling & Simulation** |
| Wire length estimation, delay modeling (Elmore delay), RLC delay, transmission line effects, and simulation techniques for interconnects. |
| **UNIT III: Signal Integrity & Crosstalk** |
| Crosstalk noise, coupling capacitance, shielding, crosstalk avoidance techniques, and power supply noise. |
| **UNIT IV: Advanced Interconnect Techniques** |
| Clock distribution networks, power distribution network design, 3D IC interconnects, and TSV (Through-Silicon Via) technology. |
| **UNIT V: Physical Design & Layout** |
| Floor planning, global interconnects, routing, and parasitic extraction in high-performance designs. . |

**Textbooks:**

**1.** Jens Lienig and Juergen Scheible**, *Fundamentals of Electronic Systems Design*, Springer, 2015**

**2.** Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu**, *VLSI Physical Design: From Graph Partitioning to Timing Closure*, Springer, 2011.**

**ReferenceBooks**:

**1.Neil H. E. Weste and David Harris**, *CMOS VLSI Design: A Circuits and Systems Perspective*, Pearson.
**2.Sung-Mo Kang and Yusuf Leblebici**, *CMOS Digital Integrated Circuits: Analysis and Design*, McGraw-Hill.
3.**Wayne Wolf**, *Modern VLSI Design: System-on-Chip Design*, Pearson.
4.**Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic**, *Digital Integrated Circuits: A Design Perspective*, Pearson.

# St.JohnsCollegeofEngineeringandTechnology
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### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## LOW POWER VLSI DESIGN

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| 25G3D57204a | PE | L | T | P | C | CIA | SEE | Total |
| | | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | Understandtheconceptsofvelocitysaturation,ImpactIonizationandHotElectronEffect |
| CO2: | ImplementLowpowerdesignapproachesforsystemlevelandcircuitlevelmeasures |
| CO3: | Designlowpoweraddersforefficientdesignofsystems. |
| CO4: | Designlowpowermultipliersforefficientdesignof systems. |
| CO5: | Designlowpowermemoriesforefficientdesignofsystems. |

| UNIT-I:Fundamentals |
|---|
| NeedforLowPowerCircuitDesign,SourcesofPowerDissipation–StaticandDynamicPowerDissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot ElectronEffect. |
| **UNIT-II:Low-PowerDesignApproaches** |
| Low-PowerDesignthrough VoltageScaling – VTCMOS circuits,MTCMOScircuits, ArchitecturalLevel Approach–Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, CircuitLevel Measures, Mask level Measures. |
| **UNIT-III:Low-VoltageLow-PowerAdders** |
| Introduction,StandardAdderCells,CMOSAdder'sArchitectures–RippleCarryAdders,CarryLook Ahead Adders, Carry SelectAdders, Carry Save Adders, Low-Voltage Low-Power Design Techniques– Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles. |
| **UNIT-IV: Low-VoltageLow-PowerMultipliers** |
| Introduction,OverviewofMultiplication,TypesofMultiplierArchitectures,BraunMultiplier,Baugh WooleyMultiplier,BoothMultiplier, IntroductionToWallaceTreeMultiplier. |
| **UNIT-V:Low-VoltageLow-PowerMemories** |
| BasicsofROM, Low-PowerROMTechnology,FutureTrendandDevelopmentofROMs,Basicsof SRAM,MemoryCell,PrechargeandEqualizationCircuit,Low-PowerSRAMTechnologies,Basicsof DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM. |

**Textbooks:**


1. CMOSDigitalIntegratedCircuits–AnalysisandDesign–Sung-MoKang,YusufLeblebici,TMH, 2011.
2. Low-Voltage,Low-PowerVLSISubsystems–Kiat-SengYeo,KaushikRoy,TMHProfessional Engineering.


**ReferenceBooks:**


1. Introduction toVLSISystems: ALogic,Circuit andSystemPerspective–Ming-BOLin, CRC Press, 2011.
2. LowPowerCMOSDesign–AnanthaChandrakasan,IEEEPress/WileyInternational,1998.
3. LowPowerCMOSVLSICircuit Design–KaushikRoy,Sharat C.Prasad,JohnWiley&Sons,2000.

# St.JohnsCollegeofEngineeringandTechnology

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### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## ALGORITHMS FOR VLSI DESIGN

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57204b | PE | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | Understand logic synthesis techniques and verification methods used in VLSI design. |
| CO2: | Analyze partitioning, placement and floor planning algorithms used in physical design automation. |
| CO3: | Apply routing algorithms for global and detailed routing in integrated circuit layout. |
| CO4: | Understand FPGA architectures and their role in modern digital system design. |
| CO5: | Apply VLSI algorithms for optimization of area, delay and power in digital circuits. |

| UNIT I – Logic Synthesis and Verification |
|---|
| Introduction to combinational logic synthesis, Boolean algebra minimization techniques, Binary Decision Diagrams (BDD), hardware models for high-level synthesis, introduction to circuit simulation and co-simulation, verification techniques in VLSI design |
| **UNIT II – Partitioning, Placement and Floor Planning** |
| Problem formulation for partitioning, classification of partitioning algorithms, Kernighan–Lin algorithm, group migration algorithms, simulated annealing techniques, placement algorithms, constraint-based floor planning, floor planning for mixed block and cell design, pin assignment techniques. |
| **UNIT III – Global Routing** |
| Problem formulation and classification of routing algorithms, maze routing algorithm, line-probe algorithm, Steiner tree based routing algorithms, Integer Linear Programming (ILP) approaches. Detailed routing: single-layer routing algorithms, two-layer channel routing algorithms, three-layer routing algorithms, switch-box routing algorithms, via minimization techniques |
| **UNIT IV – FPGA Architectures** |
| Overview of FPGA, FPGA architecture and design flow, logic blocks, programmable interconnect structures, routing architecture, programmable I/O blocks, configuration methods (SRAM, antifuse, flash), FPGA based system design |
| **UNIT V – Applications of VLSI Algorithms** |
| Technology mapping algorithms, scheduling algorithms, allocation and assignment techniques, high-level synthesis, area optimization, delay optimization, power optimization techniques in VLSI design. |

**Textbooks:**

1. **S. H. Gerez**, *Algorithms for VLSI Design Automation*, Wiley India.
2.**N. A. Sherwani**, *Algorithms for VLSI Physical Design Automation*, Springer.
3. **Sabih H. Gerez**, *Algorithms for VLSI Design Automation*, Wiley

**Reference Books:**

1. **Wayne Wolf**, *Modern VLSI Design: System-on-Chip Design*, Pearson.
2.**Neil Weste and David Harris**, *CMOS VLSI Design: A Circuits and Systems Perspective*, Pearson.
3. **Mehdi Tahoori & Sani Nassif**, *Physical Design Essentials*, Springer.
4. **Stephen Brown and Zvonko Vranesic**, *Fundamentals of Digital Logic with VHDL Design*, McGraw-Hill.

St.JohnsCollegeofEngineeringandTechnology
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# VLSI SIGNAL PROCESSING

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| 25G3D57204c | PE | L | T | P | C | CIA | SEE | Total |
| | | 3 | 0 | 0 | 3 | 40 | 60 | 100 |

## Course Outcomes:

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | StudytheexistingarchitecturessuitableforVLSI. |
| CO2: | Understandtheconceptsoffoldingandunfoldingalgorithmsandapplications. |
| CO3: | DesignnewarchitecturessuitableforVLSI. |
| CO4: | Implementfastconvolutionalgorithms. |
| CO5: | Understandtheconceptsoflowpowerdesign |

| UNIT-I:IntroductiontoDSP |
|---|
| Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and ParallelProcessingfor LowPower RetimingIntroduction,DefinitionsandProperties, SolvingSystemof Inequalities,RetimingTechniques |
| **UNIT-II:Foldingand Unfolding** |
| Folding-Introduction, FoldingTransform, Register minimizationTechniques, Register minimizationin foldedarchitectures,foldingofMultiratesystemsUnfolding-Introduction,AnAlgorithmforUnfolding, PropertiesofUnfolding,criticalPath,UnfoldingandRetiming,ApplicationsofUnfolding. |
| **UNIT-III:SystolicArchitectureDesign** |
| Introduction,SystolicArrayDesignMethodology,FIRSystolicArrays,SelectionofSchedulingVector, MatrixMultiplicationand2DSystolicArrayDesign, SystolicDesignfor SpaceRepresentationscontain Delays. |
| **UNIT-IV:FastConvolution** |
| Introduction–Cook-ToomAlgorithm–Winogardalgorithm–IteratedConvolution–CyclicConvolution– Design of Fast Convolution algorithm by Inspection |
| **UNIT-V:LowPowerDesign** |
| Digitallatticefilterstructures,bitlevelarithmetic,architecture,redundantarithmetic.Numericalstrength reduction,synchronous,waveandasynchronouspipelines,ScalingVsPowerConsumption,Power Analysis, Power Reduction techniques, Power Estimation Approaches |

**Textbooks:**

1. KeshabK.Parthi,VLSIDigitalSignalProcessing-SystemDesignandImplementation, Wiley Inter Science, 1998.
2. KungS.Y,H.J.WhileHouse,T.Kailath,VLSIandModernSignalprocessing,PrenticeHall, 1985.

**ReferenceBooks:**

1. JoseE.France,YannisTsividis,DesignofAnalog–DigitalVLSICircuits for Telecommunications and Signal Processing , Prentice Hall, 1994.
2. MedisettiV.K,VLSIDigitalSignalProcessing, IEEEPress(NY),1995

# St.JohnsCollegeofEngineeringandTechnology
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### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## CMOS MIXED SIGNAL IC DESIGN LAB

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57205 | PC | 0 | 0 | 4 | 2 | 40 | 60 | 100 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | Designandsimulateop-amp,comporatorforgivenspecifications |
| CO2: | Designandsimulatedataconverterandswitchedcapacitor circuitsforgivenspecifications |
| CO3: | DesignandsimulatePLLforgivenspecifications |
| CO4: | DesignandsimulateVCOfor given specifications |
| CO5: | UnderstandtheSignificanceofPre-LayoutSimulationandPost-LayoutSimulation |

**List ofExperiments:**

Thestudentsarerequiredtodesignandimplement theCircuit andLayout ofthefollowingExperiments using CMOS 130nm Technology.

**Cycle1:**

1) Fullycompensatedop-ampwithresistorandmillercompensation
2) Highspeedcomparatordesign
   a. Twostagecross coupledclamped comparator
   b. StrobedFlip-flop
3) Data converter

**Cycle2:**

1) Switchedcapacitorcircuits
   a. Parasiticsensitiveintegrator
   b. Parasiticinsensitiveintegrator
2) DesignofPLL
3) DesignofVCO
4) Bandgapreferencecircuit
5) Layoutsof AllthecircuitsDesignedandsimulated

**Software:**

MentorGraphics/Cadence/Tanner/IndustryEquivalentStandardSoftwareTools

**Hardware:**

PersonalComputerwithnecessaryperipherals,configurationandoperating System.

**References:**

1. DavidAjohns,KenMartin,AnalogIntegratedCircuit Design,Wiley,2008.
2. R.GregorianandG.CTernes,AnalogMOSIntegratedCircuitsforSignalProcessing,
3. Wiley,1986.
4. RoubikGregorian, IntroductiontoCMOSOpAmpand Comparators,Wiley,1999.
5. AlanHastlings, TheartofAnalogLayout,Wiley,2005.

# St.JohnsCollegeofEngineeringandTechnology
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### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## PHYSICAL DESIGN AUTOMATION LAB

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57206 | PC | 0 | 0 | 4 | 2 | 40 | 60 | 100 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | LearntheimplementationofdifferentPhysicalDesignAutomation algorithms |
| CO2: | Implementdifferentgraphalgorithms |
| CO3: | Implementdifferentpartitioningalgorithms |
| CO4: | Implementdifferentfloorplanningalgorithms |
| CO5: | Implementdifferentroutingalgorithms |

**List ofExperiments:**

**Cycle1:**

1)Graphalgorithms

a) Graphsearchalgorithms

i. Depthfirstsearch

ii. Breadthfirstsearch

b) Spanningtreealgorithm

i. Kruskal‟salgorithm

c) Shortestpathalgorithm

i. Dijkstraalgorithm

ii. Floyd-Warshallalgorithm

d) Steinertreealgorithm

2)Computationalgeometryalgorithm

a) Linesweepmethod

b) Extendedlinesweepmethod

**Cycle2:**

3)Partitioningalgorithms

a) Groupmigrationalgorithms

I. Kernighan–Linalgorithm

II. ExtensionsofKernighan-Linalgorithm

i) Fiduccias–Mattheysesalgorithm

ii) GoldbergandBursteinalgorithm

b) Simulatedannealingandevolutionalgorithms

i. Simulatedannealingalgorithm

ii. Simulatedevolutionalgorithm

III)Metricallocationmethod

4)Floorplanningalgorithms

i) Constraintbasedmethods

ii) Integerprogrammingbased methods

iii) Rectangulardualizationbased methods

iv) Hierarchicaltreebasedmethods

v) Simulatedevolutionalgorithms

vi) TimedrivenFloorplanningalgorithms

5)Routingalgorithms

I) Twoterminalalgorithms

a) Mazeroutingalgorithms

i) Lee‟s algorithm

ii) Soukup‟salgorithm

iii) Hadlock algorithm

b) Line-Probe algorithm

c) Shortestpathbasedalgorithm

II) Multiterminalalgorithm

a) Steniertreebased algorithm

i) SMSTalgorithm

ii) Z-RSTalgorithm

**Softwarerequired:**C/C++ProgrammingLanguage/Relevantsoftware

**TextBooks:**

1) NaveedShervani, AlgorithmsforPhysicalDesignAutomation,3rdEdition,Kluwer Academic,1998.
2) CharlesJAlpert,DineshP Mehta,SachinS.Sapatnekar,Hand bookofAlgorithmsfor Physical Design Automation, CRC Press,2008.

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# QUANTUM TECHNOLOGIES AND APPLICATIONS

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | Maximum Marks | | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3D57207 | MC | 2 | 0 | 0 | 2 | 40 | 60 | 100 |

**Course Outcomes:**

After the completion of the course students will be able to

| | |
|---|---|
| CO1: | Explain core quantum principles in a non-mathematical manner |
| CO2: | Compare classical and quantum information systems. |
| CO3: | Identify theoretical issues in building quantum computers |
| CO4: | Discuss quantum communication and computing concepts |
| CO5: | Recognize applications, industry trends, and career paths in quantum technology |

## UNIT 1: Introduction to Quantum Theory and Technologies

The transition from classical to quantum physics, Fundamental principles explained conceptually: Superposition, Entanglement, Uncertainty Principle, Wave-particle duality, Classical vs Quantum mechanics – theoretical comparison, Quantum states and measurement: nature of observation, Overview of quantum systems: electrons, photons, atoms, The concept of quantization: discrete energy levels, Why quantum? Strategic, scientific, and technological significance, A snapshot of quantum technologies: Computing, Communication, and Sensing ,National and global quantum missions: India's Quantum Mission, EU, USA, China

.

## UNIT 2: Theoretical Structure of Quantum Information Systems

What is a qubit? Conceptual understanding using spin and polarization, Comparison: classical bits vs quantum bits, Quantum systems: trapped ions, superconducting circuits, photons (non-engineering view),Quantum coherence and decoherence – intuitive explanation, Theoretical concepts: Hilbert spaces, quantum states, operators – only interpreted in abstract,The role of entanglement and non-locality in systems, Quantum information vs classical information: principles and differences,Philosophical implications: randomness, determinism, and observer role

## UNIT 3: Building a Quantum Computer – Theoretical Challenges and Requirements

What is required to build a quantum computer (conceptual overview)?,Fragility of quantum systems: decoherence, noise, and control, Conditions for a functional quantum system: Isolation, Error management, Scalability, Stability, Theoretical barriers:
Why maintaining entanglement is difficult,Error correction as a theoretical necessity, Quantum hardware platforms (brief conceptual comparison),Superconducting circuits, Trapped ions, Photonics, Visionvs reality: what's working and what remains elusive,The role of quantum software in managing theoretical complexities

## UNIT 4: Quantum Communication and Computing – Theoretical Perspective

Quantum vs Classical Information, Basics of Quantum Communication, Quantum Key Distribution (QKD),Role of Entanglement in Communication,The Idea of the Quantum Internet – Secure Global Networking,Introduction to Quantum Computing,Quantum Parallelism (Many States at Once),Classical vs Quantum Gates, Challenges: Decoherence and Error Correction,Real-World Importance and Future Potential

.

| UNIT 5: Applications, Use Cases, and the Quantum Future |
|---|
| Real-world application domains: Healthcare (drug discovery),Material science, Logistics and optimization, Quantum sensing and precision timing, Industrial case studies: IBM, Google, Microsoft, PsiQuantum,Ethical, societal, and policy considerations, Challenges to adoption: cost, skills, standardization,Emerging careers in quantum: roles, skillsets, and preparation pathways,Educational and research landscape – India's opportunity in the global quantum race |

**Textbooks**:

1. Michael A. Nielsen, Isaac L. Chuang, *Quantum Computation and Quantum Information*, Cambridge University Press, 10th Anniversary Edition, 2010.
2. Eleanor Rieffel and Wolfgang Polak, *Quantum Computing: A Gentle Introduction*, MIT Press, 2011.
3. Chris Bernhardt, *Quantum Computing for Everyone*, MIT Press, 2019.

**Reference Books**:

1. David McMahon, *Quantum Computing Explained*, Wiley, 2008.
2. Phillip Kaye, Raymond Laflamme, Michele Mosca, *An Introduction to Quantum Computing*, Oxford University Press, 2007.
3. Scott Aaronson, *Quantum Computing Since Democritus*, Cambridge University Press, 2013.
4. **Alastair I.M. Rae**, *Quantum Physics: A Beginner's Guide*, Oneworld Publications, Revised Edition, 2005.
5. **Eleanor G. Rieffel, Wolfgang H. Polak**, *Quantum Computing: A Gentle Introduction*, MIT Press, 2011.
6. **Leonard Susskind, Art Friedman**, *Quantum Mechanics: The Theoretical Minimum*, Basic Books, 2014.
7. **Bruce Rosenblum, Fred Kuttner**, *Quantum Enigma: Physics Encounters Consciousness*, Oxford University Press, 2nd Edition, 2011.
8. **GiulianoBenenti, GiulioCasati, GiulianoStrini**, *Principles of Quantum Computation and Information, Volume I: Basic Concepts*, World Scientific Publishing, 2004.
9. **K.B. Whaley et al.**, *Quantum Technologies and Industrial Applications: European Roadmap and Strategy Document*, Quantum Flagship, European Commission, 2020.
10. **Department of Science & Technology (DST), Government of India**, *National Mission on Quantum Technologies & Applications – Official Reports and Whitepapers*, MeitY/DST Publications, 2020 onward.

**Online Learning Resources**:

- IBM Quantum Experience and Qiskit Tutorials
- Coursera – Quantum Mechanics and Quantum Computation by UC Berkeley
- edX – The Quantum Internet and Quantum Computers
- YouTube – Quantum Computing for the Determined by Michael Nielsen
- Qiskit Textbook – IBM Quantum

St.JohnsCollegeofEngineeringandTechnology
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# AUDIT COURSE-II

# St.JohnsCollegeofEngineeringandTechnology
## (AUTONOMOUS)
### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## PEDAGOGY STUDIES

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| 25G3DAC201a | AC | L | T | P | C | CIA | SEE | Total |
| | | 2 | 0 | 0 | 0 | 40 | 0 | 40 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | Whatpedagogicalpracticesarebeingusedbyteachersinformalandinformalclassroomsin developingcountries? |
| CO2: | Whatistheevidenceontheeffectiveness ofthesepedagogicalpractices,inwhat conditions,andwithwhatpopulationoflearners? |
| CO3: | Howcanteachereducation(curriculumandpracticum)andtheschoolcurriculumand guidancematerialsbestsupporteffectivepedagogy? |
| CO4: | Learnalignmentwithclassroompracticesandfollow-up support |
| CO5: | UnderstandtheResearchgapsandfuturedirections |

| UNIT-I |
|---|
| **IntroductionandMethodology:**Aimsandrationale, Policybackground, Conceptualframeworkand terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and Searching. |
| **UNIT-II** |
| **Thematic overview:** Pedagogical practices are being used by teachers informal and informal classrooms in developing countries. Curriculum, Teacher education |
| **UNIT-III** |
| Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment ofincludedstudies. Howcanteacher education(curriculumandpracticum)andtheschool curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and natureof thebody of evidencefor effectivepedagogical practices. Pedagogic theory and pedagogical approaches.Teachers'attitudesandbeliefsandPedagogicstrategies. |
| **UNIT-IV** |
| **Professionaldevelopment:**alignment withclassroompracticesandfollow-upsupport,Peer support, Support from the head Teacherandthecommunity.Curriculumandassessment,Barrierstolearning:limitedresourcesandlarge classsizes |
| **UNIT-V** |
| **Researchgapsandfuturedirections:** Researchdesign**,**Contexts**,**Pedagogy**,**Teachereducation**,** Curriculum and assessment**,** Dissemination and research impact. |

**Suggested Reading:**


1. AckersJ,HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare, 31(2):245-261.
2. AgrawalM(2004)Curricularreforminschools:Theimportanceofevaluation,Journalof
3. CurriculumStudies,36(3):361-379.
4. AkyeampongK(2003)TeachertraininginGhana-doesitcount?Multi-siteteacher education research project (MUSTER) country report 1. London: DFID.
5. AkyeampongK,LussierK,PryorJ,WestbrookJ(2013)Improvingteachingand learning of basic maths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
6. AlexanderRJ(2001)Cultureandpedagogy:Internationalcomparisonsinprimary

education.OxfordandBoston:Blackwell.
7. ChavanM(2003)ReadIndia:Amassscale,rapid,‘learningtoread’campaign.
8. www.pratham.org/images/resource%20working%20paper%202.pdf.

# St.JohnsCollegeofEngineeringandTechnology
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## STRESS MANAGEMENT BY YOGA

| IM.Tech–IISemester | | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | | |
| 25G3DAC201b | AC | L | T | P | C | CIA | SEE | Total |
| | | 2 | 0 | 0 | 0 | 40 | 0 | 40 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | UnderstandtheDefinitionsofEightpartsofyoga |
| CO2: | LearnaboutYamand Niyam |
| CO3: | LearnDo`sandDon't'sinlife |
| CO4: | PracticeAsanand Pranayam |
| CO5: | Develophealthymindinahealthybodythusimprovingsocialhealthalso Improveefficiency |

| UNIT-I |
|---|
| Definitions ofEightpartsofyoga.(Ashtanga) |
| **UNIT-II** |
| YamandNiyam. |
| **UNIT-III** |
| Do`sandDon't'sinlife.<br>i) Ahinsa,satya,astheya,bramhacharyaandaparigrahaii)Shaucha,santosh,tapa,swadhyay, ishwarpranidhan |
| **UNIT-IV** |
| Asanand Pranayam |
| **UNIT-V** |
| i)Variousyogposesandtheirbenefitsformind&bodyii)Regularizationofbreathingtechniquesandits effects-Types of pranayam |

**Suggested Reading:**

1. 'Yogic AsanasforGroupTarining-Part-I":JanardanSwamiYogabhyasiandal, Nagpur 2."Raja yogaorconquering the Internal Nature" by Swami Vivekananda, Advaita

2. Ashrama(PublicationDepartment),Kolkata

# St.JohnsCollegeofEngineeringandTechnology
## (AUTONOMOUS)
### DEPARTMENTOFELECTRONICSANDCOMMUNICATIONENGINEERING

## PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS

| IM.Tech–IISemester | | | | | | | SJCET-R25 |
|---|---|---|---|---|---|---|---|
| CourseCode | Category | Hours/Week | | | Credits | MaximumMarks | |
| | | L | T | P | C | CIA | SEE | Total |
| 25G3DAC201c | AC | 2 | 0 | 0 | 0 | 40 | 0 | 40 |

**Course Outcomes:**

After thecompletionofthecoursestudentswillbeableto

| | |
|---|---|
| CO1: | StudyofNeetisatakam-Holisticdevelopmentofpersonality(Part-1) |
| CO2: | StudyofNeetisatakam-Holisticdevelopmentofpersonality(Part-2) |
| CO3: | Shrimad-Bhagwad-Geetawillhelpthestudentindevelopinghispersonalityandachieve the highest goal in life |
| CO4: | Thepersonwho hasstudiedGeetawillleadthenationandmankindtopeaceandprosperity |
| CO5: | StudyofNeetishatakamwillhelpindevelopingversatilepersonalityofstudents |

| UNIT-I |
|---|
| Neetisatakam-Holistic development of personalityVerses-19,20,21,22(wisdom)<br><br>Verses-29,31,32(pride&heroism)<br>Verses-26,28,63,65(virtue) |
| **UNIT-II** |
| Neetisatakam-Holistic development of personalityVerses-52,53,59(dont's)<br>Verses-71,73,75,78(do's) |
| **UNIT-III** |
| Approachtodaytoday workandduties.<br>ShrimadBhagwadGeeta:Chapter2-Verses41,47,48,Chapter3-Verses13,21,27,35,Chapter6-Verses5,13,17,23,35,<br>Chapter18-Verses45,46,48. |
| **UNIT-IV** |
| Statementsofbasicknowledge.<br>ShrimadBhagwadGeeta:Chapter2-Verses56,62,68Chapter12 - Verses13,14,15,16,17,18<br>PersonalityofRolemodel.ShrimadBhagwad Geeta: |
| **UNIT-V** |
| Chapter2-Verses17,Chapter3-Verses36,37,42,<br>Chapter4-Verses18,38,39<br>Chapter18–Verses37,38,63 |

**Suggested Reading:**

1. "Sri mad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (Publication Department), Kolkata
2. Bhartrihari's Three Satakam (Niti-sringar-vairagya) by P.Gopinath, Rashtriya Sanskrit Sansthanam, New Delhi.